**MEng Design Project Announcement – 2018-19**

**Project Title:** Design and Evaluation of a RISC-V Vector Unit

**Brief Description of Design Project Goals:**

**Overview:**
RISC-V is a new open instruction set architecture that is growing in popularity across both industry and academia. RISC-V was explicitly designed to enable specialized extensions for various application domains. For example, the RISC-V vector extensions are designed to accelerate high-performance numerical computing. More information about these extensions was presented at a RISC-V workshop last spring:

- [https://goo.gl/iPxxej](https://goo.gl/iPxxej)
- [https://www.youtube.com/watch?v=S4fxBZD79gc](https://www.youtube.com/watch?v=S4fxBZD79gc)
- [https://goo.gl/KNbM1u](https://goo.gl/KNbM1u)
- [https://www.youtube.com/watch?v=ESu9NI3h1Y4](https://www.youtube.com/watch?v=ESu9NI3h1Y4)

The goal of this MEng design project is to design, implement, verify, and evaluate a RISC-V vector unit at the register-transfer level suitable for mapping to an ASIC. The student will have access to a state-of-the-art commercial standard-cell-based toolflow and the PDK for an advanced technology node for evaluating the area, energy, and timing of the vector unit. Near the end of the project, the student will compose the vector unit with a scalar processor and memory system to conduct a more complete evaluation.

**Specific MEng Contribution:**
The student(s) will work closely with PhD students currently exploring various accelerator architectures. A tentative list of tasks includes: (1) specify the subset of the RISC-V vector instruction set to be implemented; (2) implement an initial single-lane baseline design; (3) implement a more sophisticated multi-lane alternative design; (4) develop an effective testing strategy to ensure the functional correctness of all designs; and (5) conduct a broad design-space exploration of the vector unit. Weekly meetings with the field advisor will be held to assess progress; note that insufficient progress after the fall semester will likely result in canceling the project.

**ECE Field Advisor:**
- **Name** – Christopher Batten
- **Email** – cbatten@cornell.edu
- **Phone** – 607-255-2672
- **Office** – 323 Rhodes Hall

**Number of MEng Students Needed:**

One to two students.
Required Skills:

- Self-motivation and the ability to independently research an engineering design problem
- Experience with standard software-engineering best practices including version source control, test-driven development, and object-oriented programming (e.g., CS 2110 or ECE 2400)
- Experience with Unix/Linux and using command-line interfaces
- Experience with vector engines and/or ASIC design is a strong plus but not required

Estimated Project Time Frame:

Fall 2018 and Spring 2019 semesters

Application Procedure

Interested students are strongly encouraged (although not required) to enroll in ECE 4750. Applicants should email a cover letter, resume, and unofficial transcript to cbatten@cornell.edu if they are interested. The cover letter should highlight the applicant's qualifications, why the applicant is interested in this project, and the courses they intend to take in the fall and spring semesters. Your resume should highlight course work, industry experience, and extracurricular activities relevant to the project. Strong candidates will be contacted for a one-on-one meeting with the field advisor.