Computer Systems Q Exam Areas

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Note: It is not enough just to be able to describe concepts; you will need to be able to apply concepts in new contexts, and also be able to evaluate design alternatives.

1 VLSI Area

VLSI General: Moore's Law; Kryder's Law; Koomey's Law.

Boolean Algebra: Axioms and main theorems of Boolean algebra; combinational logic minimization: Algebraic simplification, Karnaugh maps, don't-cares, races.

MOSFET: P-N junction and diodes; operation regimes; body effect; short-channel effects; parasitic capacitances; switch model; pass transistors and transmission gates.

CMOS Inverter: Voltage transfer characteristics; operation regimes; regenerative property and noise margins; latch-up; dynamic behavior; propagation delay; sizing (logical effort).

Static CMOS: Pull-up and pull-down networks; CMOS gate synthesis and analysis; standard-cell design; stick diagrams and Euler path; timing characteristic (worst/best case delay, rise/fall times); gate sizing (logical effort); pass-transistor (PT) logic; transmission-gate (TG) logic.

Dynamic Logic: Dynamic CMOS; domino logic; np-CMOS, zipper, and NORA logic.

Sequential Logic: D-latch and SR-latch; master-slave D-flip-flop; timing of latches and flip-flops (setup/hold times); timing analysis (max. clock frequency, critical path, clock skew); race conditions.

Energy/Power Consumption: Static CMOS power consumption; dynamic CMOS power consumption; statistical power analysis; low-power design techniques; voltage-frequency scaling; leakage reduction.

Architecture Transforms: Area/delay trade-off; pipelining; retiming; replication; iterative decomposition; time sharing.

Adder Circuits: Full adder (various designs); ripple-carry adder; Manchester-carry chain; carry-skip adder; carry-select adder; carry-save adder (CSA); carry-lookahead adder (CLA).

Arithmetic/Logic Circuits: Two's complement/sign magnitude numbers; shifters and rotator circuits; comparator circuits; n-input multiplexers; array and CSA multipliers.

Memories and ROMs: NAND and NOR ROM; SRAM (design and sizing of 6T cells); DRAM (3T and 1T cells); NAND/NOR row decoders; precharge circuitry; sense amplifiers.

Wire Models: RC model; fringing capacitance; wire parasitics and crosstalk; Elmore delay; IR drop.

2 Architecture Area

Processors (basic): Instruction set architectures; single-cycle processor datapath and control unit; hard-wired vs. microcoded FSM processors; pipelined processors; resolving structural, data, control, and name hazards; handling exceptions; analyzing processor performance (iron law of processor perf.); transition from CISC to RISC.

Memories: Memory technology (registers, register files, SRAM, DRAM); spatial vs. temporal locality; direct-mapped vs. associative caches; write-through vs. write-back caches; replacement policies; FSM caches; parallel-read, pipelined-write caches; integrating processors and caches; analyzing memory performance (avg. memory access latency); page table, TLB; virtually vs. physically addressed/tagged caches; cache coherence, MSI; memory consistency; locks, barriers.

Networks: Torus and butterfly topologies; routing algorithms; channel and router microarchitecture; traffic patterns; integrating processors, caches, and networks; analyzing network performance (ideal throughput, zero-load latency).

Processors (advanced): Superscalar execution; out-of-order execution: scoreboard, issue queue, reorder buffer, handling exceptions; register renaming: pointer-based, value-based schemes; memory disambiguation: finished-store buffer, finished-load buffer, load/store queues, in-order vs. out-of-order load/store issue; branch prediction: software-based, predication, one-level and two-level branch-history tables, tournament predictors, branch-target buffer, return address stack; speculative execution; VLIW processors: loop unrolling, software pipelining; SIMD processors: subword-SIMD, vector-SIMD; multithreaded processors: vertical multithreading, simultaneous multithreading.

Boolean Algebra: Axioms and main theorems of Boolean algebra; combinational logic minimization: Algebraic simplification, Karnaugh maps, don't-cares, races.

Combinational Blocks: Mux, demux, decoder, encoder; carry-propagate adder, carry-save adder, carry-lookahead adder; integer multiplication.

Sequential Logic: D-latch and SR-latch; master-slave D-flip-flop; timing of latches and flip-flops (setup/hold times); timing analysis (max. clock frequency, critical path, clock skew); race conditions; FSMs; Mealy and Moore automata; sequential logic design; registers, counters, timers; communicating FSMs.

3 Systems Area

Programs: Instruction set architectures: instruction encoding, register organization, endianness, control flow; compiling, linking, and loading.

Calling conventions and Stack: Parameter-passing conventions; stack structure; stack frame.

Interrupts and Exceptions: Polling; interrupts; exceptions; software traps; system calls.

Process Management: Time-sharing; context switching; scheduling: FCFS, round-robin, priority, SJF; aperiodic real-time: EDD/EDF; periodic real-time: timeline scheduling; rate-monotonic scheduling; interprocess communication.

Memory Management and Storage Memory protection, translation, and virtualization: base/bound, pagination, segmentation; TLB; virtual memory; memory allocation; basic I/O; storage.

Concurrency: Critical sections; atomicity; mutual exclusion, progress, fairness; locks and monitors; RMW operations, t&s; ticket lock; semaphores; wait/signal; Hoare vs. Mesa semantics; readers and writers; producers and consumers; priority inversion, PIP, PCP.

Networking: Physical networking: Wireless, modulation, circuit- and packet-switched, mobile networks; data link: sliding window, error correcting codes; medium access: aloha, ethernet, wireless LANs, bridging; network layer: routing, congestion control, QoS; transport layer: sockets, UDP, TCP, delay tolerant networking; application layer: DNS, Email, WWW, streaming audio/video; security: basic crypto, symmetric key algorithms, public key, digital signatures, key management, firewalls/IPSec, authentication protocols, web security (SSL).